IN THE SPECIFICATION:

Please amend paragraph **[0009]** as follows:

[0009] One of the problems associated with conventional lead frame configurations is that with the decreasing size of the semiconductor die and the increasing amount of circuitry included in the semiconductor die, it is necessary to connect an ever-increasing number of bond pads on the active surface of the semiconductor die with an ever-increasing number of lead fingers of the lead frame. This requires that the bond pads on the semiconductor die be located on smaller pitch spacings and the width of the lead fingers be smaller. This, in turn, leads to smaller wire bonds on both the bond pads of the semiconductor die and the lead fingers of the lead frame, which causes the wire bonds to be more highly stressed by the forces placed on them. This stress placed on the wire bonds requires that the metal of the bond pad, to which the wire bond is to be made, be highly susceptible to wire bonding and the formation of high strength wire bonds therewith when using well-known wire material, such as gold, ~~etc.~~ etc., and standard or conventional wire bonding equipment.

Please amend paragraph **[0028]** as follows:

[0028] Referring to drawing FIG. 2E, a portion of a semiconductor device 10 is shown having a bond pad 12 thereon with the copper layer base 12′ located thereon having the upper surface thereof located at approximately the same level as the active surface 14 of substrate 11 of the semiconductor device 10, the active surface 14 having a layer of insulating material 13 (typically a passivation layer of an insulating oxide or insulating nitride) thereon. As illustrated in drawing FIG. 2E, the copper layer base 12′ of bond pad 12 has a barrier layer 12‴ formed of a suitable material having a suitable metal layer 12″ selectively plated thereon using well-known plating processes. The function of the barrier layer 12‴ is to help prevent interaction between the copper layer base 12′ and the suitable metal layer 12″ of the bond pad 12 and/or to help prevent or decrease the growth of intermetallics between the copper layer base 12′ and the metal layer 12″. For instance, barrier materials, such as titanium, tungsten, tantalum, nickel, tantalum-nickel alloys, titanium-nickel alloys, titanium-tungsten alloys, ~~etc.~~ etc., are frequently

used in conjunction with aluminum alloy interconnects. In other instances, a barrier layer of nickel between copper and tin will decrease the growth of tin-copper intermetallics. The layers of metal forming the bond pads 12 also occasionally are silicided, or have a refractory interconnect material, such as molybdenum, tungsten, or tungsten silicide, as part thereof. The function of the metal layer 12″ is to provide a good metal to which an effective wire bond may be formed using well-known wire bonding apparatus, such as a metal layer 12″ of gold ~~when~~ when a gold wire 20 is being used for wire bonding.

Please amend paragraph **[0039]** as follows:

[0039] Referring to drawing FIG. 5B, a process 200 for the formation of a bond pad 12 including a copper layer base 12′ and a layer of metal 12″ thereon for wire bonding purposes as described hereinbefore is illustrated. As illustrated in step 202, a substrate 11 as described hereinbefore for a semiconductor device 10 has a layer of copper or copper alloy deposited thereon using any desired deposition process. Subsequently, in step 204, the copper layer base 12′ is patterned and etched to form the desired shape, number, and pattern for the bond pads 12 on the active surface 14 of the substrate 11 of the semiconductor device 10. Then, in step 206, the layer of metal 12″ is deposited on the copper layer base 12′ using any desired deposition process, as described hereinbefore, such as electrodeposition, electroless deposition, ~~etc.~~ etc., to form the bond pad 12 having a copper layer base 12′ and layer of metal 12″ thereon for good wire bonding properties. A layer of insulating material 13 is typically applied to the active surface 14 of the substrate 11 to protect the circuitry formed thereon of the semiconductor device 10. After the completion of the semiconductor device 10 having bond pads 12 including a copper layer base 12′ and layer of metal 12″ thereon, the semiconductor device 10 may be assembled to a lead frame (not shown) for wire bonding a wire 20 to the bond pad 12 of the semiconductor device 10 using any suitable wire bonding process 208 and apparatus.

Please amend paragraph **[0045]** as follows:

[0045] Referring to drawing FIG. 5G, a process 700 for the formation of a bond pad 12 including a copper layer base 12′ and a layer of metal 12″ thereon for conductive lead 23 of TAB tape 21 bonding purposes as described hereinbefore is illustrated. As illustrated in step 702, a substrate 11 as described hereinbefore for a semiconductor device 10 has a layer of copper or copper alloy deposited thereon using any desired deposition process. Subsequently, in step 704, the copper layer base 12′ is patterned and etched to form the desired shape, number, and pattern for the bond pads 12 on the active surface 14 of the substrate 11 of the semiconductor device 10. Then, in step 706, the layer of metal 12″ is deposited on the copper layer base 12′ using any desired deposition process, as described hereinbefore, such as electrodeposition, electroless deposition, ~~etc.~~ etc., to form the bond pad 12 having a copper layer base 12′ and layer of metal 12″ thereon for good wire bonding properties. A layer of insulating material 13 is typically applied to the active surface 14 of the substrate 11 to protect the circuitry formed thereon of the semiconductor device 10. After the completion of the semiconductor device 10 having bond pads 12 including a copper layer base 12′ and layer of metal 12″ thereon, the semiconductor device 10 may be assembled to a conductive lead 23 of a TAB tape 21 for wire bonding a conductive lead 23 to the bond pad 12 of the semiconductor device 10 using any suitable bonding process 708 and apparatus.